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EP 0805356 A2 EP 0277764 A2

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H1K KMA
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(54) Abstract Title

A semiconductor die structure incorporating a capacitive sensing probe

(57) The die element (8) has active-circuit elements and a capacitative testing probe (18) carried by the die is conductively linked to a terminal connection point. The probe is insulated from the active circuit elements and their associated metallisation, and can itself be formed as part of the semiconductor or as a metallisation or deposit of conductive material. Greater sensitivity and improved 'line of sight' for capacitative testing is obtained.

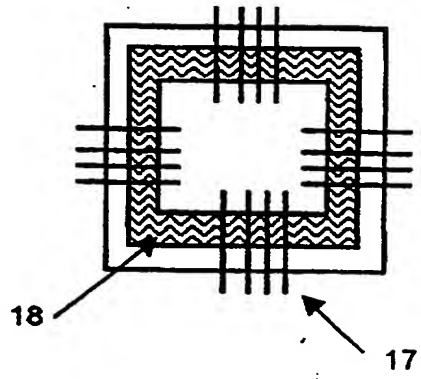

FIG.4

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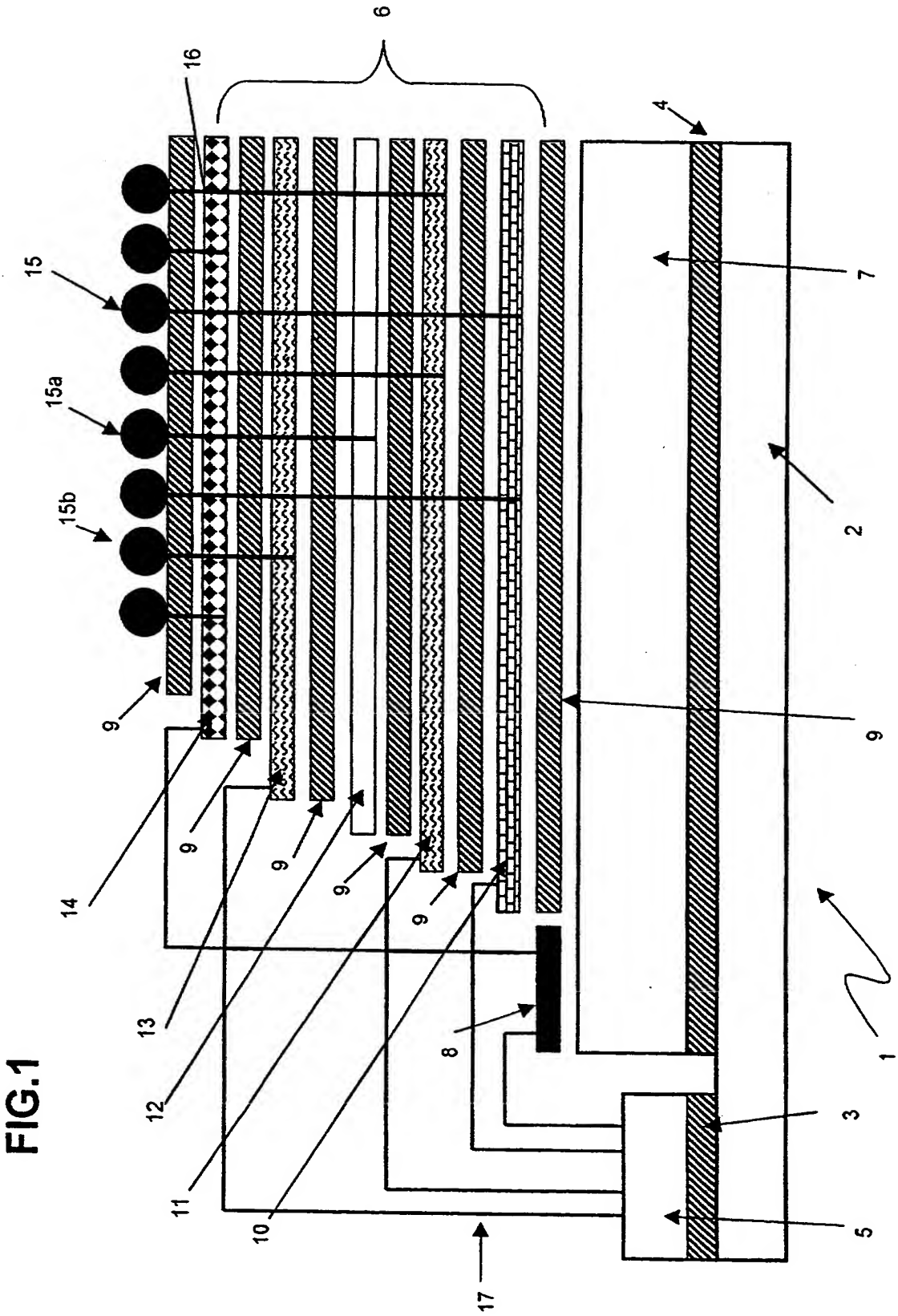

FIG.1

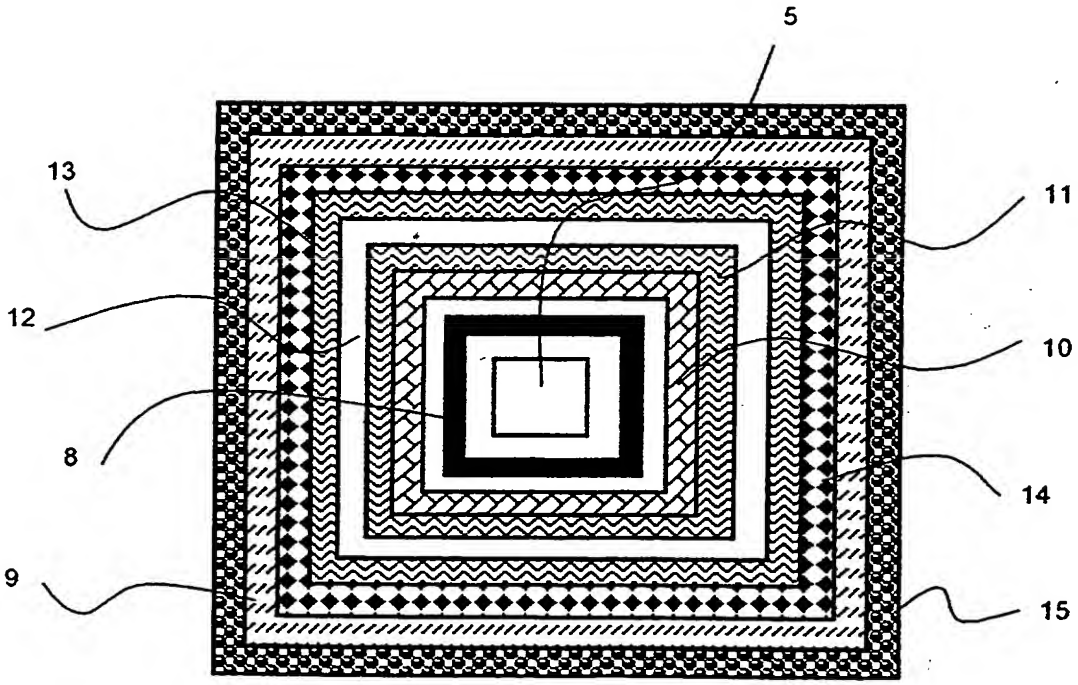

FIG.2

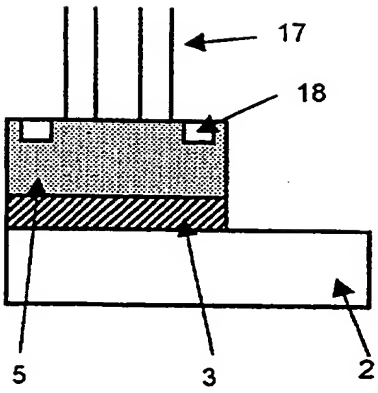

FIG.3

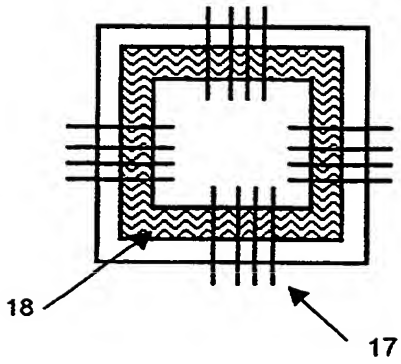

FIG.4

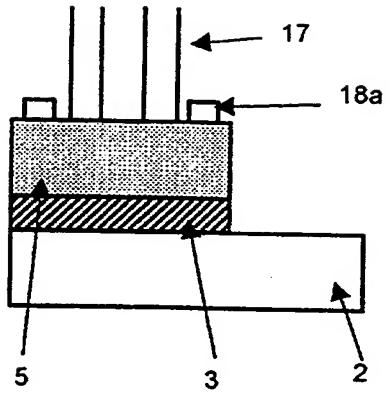

FIG.5

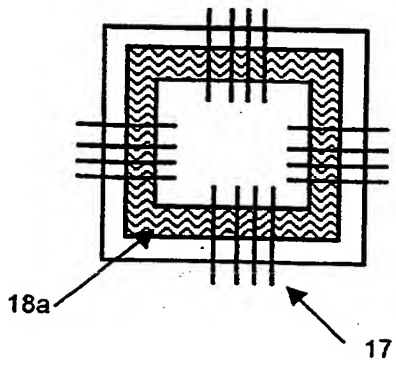

FIG.6

DIE MOUNTED CAPACITATIVE SENSING AND BOND TESTING

Field of the Invention

This invention relates to semiconductor die structures. It also relates to packaged, die structures and related electronic circuits.

Background to the Invention

Fabrication of semiconductor components falls broadly into two stages. First is the fabrication of the semiconductor die and its associated metallisation. This is followed by mounting and electrical connection of the die to some kind of package that is suitable for handling and incorporation into larger circuit structures. Packages may include lead frames or other structures that have leads or terminals extending outwardly from the package. Other structures may have the outer terminals in the form of a grid of balls.

Packages may include other elements of circuitry, for example as in a multi-layer electronic device package in which a semiconductor die is mounted alongside a multi-layer stack that includes printed or integrated circuit layers (often called 'signal' layers), a ground and/or power plane and a ball grid array. These various conductive layers are separated by insulating layers and the balls of the array interconnect by way of vertical traces extending through vias to the individual parts or layers to which they make predetermined contact.

An important adjunct to the packaging process is the testing of the circuits and package connections. This is particularly relevant for more complex packages. Various methods have been devised. One method, generally known as "vector testing", requires application of large sets of binary signals (vectors) to the input terminals of the circuit and retrieval of relevant sets of outputs. For circuits of any complexity, the vector testing mode is complex and often lengthy. Further, it has a general disadvantage that the output vectors do not

necessarily indicate directly the nature and location of a fault that causes deviation from the vector values expected from a correctly functioning circuit.

Another known form of testing is described, for example, in United States patent US-5274336. This is a capacitative method in which a plurality of spring loaded conductive probes (known as a "bed of nails") make ohmic contact, selectively, to the input and output pins on one surface of a multi-layer device while a capacitative probe constituted by an external plate is suspended over or held separate from the circuit. The capacitance between a selected pin and the probe can then be measured by stimulation from an AC source. This technique is useful for in-circuit testing because differences between expected capacitance and measured capacitance indicate faults. If a pin does not make adequate connection with the printed circuit due to inadequate soldering, then there is a reduction of capacitance in series with the capacitance formed with the capacitative probe, and this change can readily be detected.

This capacitative sensing technique does not require knowledge of the core functionality of the device, depends only on the physical properties of the packaging and is in general simpler and more rapid than vector testing. However it can prove difficult to obtain accurate and always meaningful results, for example if the device includes a ground plane or heat spreader which is not electrically isolated from other planes in the device. Under these circumstances their influence can swamp or interfere with the measurements linked to the external capacitative probe. This is particularly the case with multi-layer structures that have ball grid array external connection where 'line of sight' from the probe to the desired conductive element is more likely to be obscured by virtue of the vertical stacking arrangement, than with structures having laterally extending leads.

A way of overcoming this latter problem proposed in a copending application is to utilise a conductive layer within the multi-layer structure. This means that the capacitative sensing plane can be located adjacent (except for insulator) a signal plane and not blocked by a ground or power plane or heat spreader. The sensing plane can be connected or tracked

internally to an accessible connection such as a solder ball. In instances where a spare plane is available, this technique could prove useful. However in many instances there is not a spare plane available and new packaging would have to be manufactured and tested with that attendant overhead.

Summary of the Invention

The present invention has as its main object a new construction enabling improved vectorless testing techniques in general and improvements to capacitatively coupled testing in particular.

The invention is based on the location of a capacitative sensor probe element, such as a plate or channel, either in the semiconductor die element itself or in its metallisation. Existing fabrication stages may be utilised in providing the probe. This provides a stable in-package location without blocking problems and without package redesign. A further advantage is achieved in that capacitative coupling to the die bond wires may also be sensed and checked and greater accuracy is achieved because the sense point is at the trace start point. The technique is applicable to all package types, with or without lead frames, but is particularly useful in layered or stacked package configurations that do not have laterally extending external conductive elements.

Brief Description of the Drawings

The invention is illustrated, by way of example, in the accompanying drawings in which:

Figure 1 illustrates schematically, in simplified form and not to scale, a cross-section through a multi-layer circuit device of typical general structure;

Figure 2 illustrates schematically, in simplified form, a plan layout of a multi-layer circuit of the general structure shown in Figure 1;

Figure 3 illustrates schematically in cross-section, the die and immediate surrounds from Figure 1, modified in accordance with a first embodiment of the invention;

Figure 4 illustrates schematically in plan-view the die and immediate surrounds from Figure 1 modified in accordance with the first embodiment of the invention;

Figure 5 illustrates schematically in cross-section, the die and immediate surrounds from Figure 1, modified in accordance with a second embodiment of the invention;

Figure 6 illustrates schematically in plan-view the die and immediate surrounds from Figure 1, modified in accordance with a second embodiment of the invention.

Detailed Description of Preferred Embodiments

Figures 1 and 2 illustrate respectively the general structure of a packaged multi-layer electronic circuit device. The invention is described in the context of this type of package as they have proved problematical to test because of blocking planes. The particular package illustrated is an example only, the package shape, detail and layer constructions may vary according to design requirements. Multi-die packages may also be constructed, and the technique described in relation to the multi-layer package can be applied in any situation or type of packaging for example with compact or ball type terminals or with leads or pins.

In Figure 1, the packaged device shown, indicated generally by reference 1, consists of a single die element 5 mounted in a package that includes multiple conductive layers that are connected to the die. Within the context of this specification, 'die element' includes the die or the die and its associated metallisation. For clarity the multiple conductive layers are shown, in section, only on one side of the die, but as can be seen from the plan view of

Figure 2 a more common arrangement is for the die to be mounted centrally and for the layer structure to extend around the die. Some of the layers may be side by side or a single layer and others in a stack with intervening insulating layers.

The particular arrangement illustrated has a conductive heat spreader 2 on to which are mounted by way of respective adhesive layers 3 and 4, the die element 5 and a multi-layer stack 6.

The multi-layer stack has at its base a cavity 7, made for example of copper, on to which proximate the die is a ground or power ring 8. Alongside the ground ring 8 is the first of a series of insulating layers 9 which interleave with conductive layers. In alternative structures the ring 8 may extend further outwards beneath the stack with an insulating layer on top. The conductive layers have differing functions, typically the first layer 10 being a power layer, which has a layout of the power rail (e.g.Vcc) for the various circuits, this being followed by a stack of signal layers 10, 11, 12, 13 and an uppermost ground layer or plane 14. On top of the final insulating layer 9 that over lies the ground plane 14 there is a ball grid array 15.

As shown, individual ones of the solder balls connect by way of vertical traces 16 to predetermined points on predetermined ones of the conductive planes. For example solder ball 15a connects to signal plane 12 and solder ball 15b connects to signal plane 13 The traces 16 pass through vias in the insulating layers 9 and usually only connect at their termination.

Conductive leads 17 extend from the die to the conductive planes. These leads are usually in the form of bond wires.

In the event that one of the signal layers is not actively or fully utilised in the device function, say for example layer 12, it can be utilised as a sensing layer in capacitatively

coupled testing. However, such availability is not always present and other package types and layouts may not have such possibilities.

Turning now to Figure 3, this shows just the die 5, modified in accordance with the invention, and its immediate surrounds of heatspreader 2, adhesive 3 and bond wires (leads) 17. The die has a channel 18 which is filled with a conductive material, which may be silicon, polysilicon, metallisation or compounds, and which is connected to be utilised as a capacitative probe element in capacitative testing. It will be appreciated that various active circuits elements such as transistors will be fabricated within the die and connect to bond pads for onward interconnection.

Referring to Figure 4, the layout of the channel 18 from above can be viewed. From this it can be observed that due to the generally peripheral and continuous nature of the particular channel configuration illustrated, all the bond wires have to cross over the channel. This type of configuration yields particular advantage in that good capacitative linkage with the bond wires is thereby achieved.

Other channel layouts are possible, as indeed are other locations where the "real estate" permits. Layouts need not create a continuous ring structure. What is required is that the signals or traces to be verified using capacitative sensing have a clear 'sight' of the probe without an intervening (conductive) ground or power plane. Consideration may also be given to the area required to obtain sufficient linkage.

Figures 5 and 6 show a variation in which a similar layout pattern for the capacitative probe element is disposed on, rather than in, the die element. In this instance the capacitative probe element 18a is a track of metallisation, or other conductive material. The capacitative track 18a may conveniently be formed as part of the die metallisation process, either in the same plane as other metallisation or in a separate layer.

As with the Figure 4 embodiment, the illustrated layout achieves good capacitative linkage to the die bond wires which in turn link conductively to the signal layers. Other layouts are also possible, where real estate permits. Given the additional flexibility that can be achieved through layering, larger areas may be utilised, possibly even extending to cover the entire die top surface, the bonding and other design considerations permitting.

In both the described embodiments, in particular the latter, it may also be possible to utilise separately or in combination different surfaces of the die to fit in with layout or to maximise surface area used. Utilising the semiconductor substrate side (or back) of the die may be particularly useful in flip-chip type mountings. It is not essential for the bond wires to cross over the probe, although this can provide advantages in capacitative linkage. Other considerations, such as wire sweep, may indicate location of the probe more towards the interior of the die surface.

The capacitative sensing probe element 18 or 18a while remaining insulated from surrounding active circuit elements and their interconnections must itself be capable of conductive linkage to the outside of the package. This may start with a bond pad or a trace on the die and then continue to an external terminal element by any available route, which may vary according to design. Usually it will be by die bond wires and package or substrate routing to any spare solder ball, or to a conductive surface of the packaged device which is thereby specifically utilised for capacitative vectorless testing. This may include routing to the heat spreader. From its solder ball, conductive link or other terminal, the conductive sensor ring (or other sensor element shape) can be integrated into an in-circuit test fixture.

Due to the integral fabrication of the sensor probe element, that is the probe being part of or carried by (on or in) the die, an amplifier circuit for the capacitative testing may be incorporated into the die device, thereby eliminating the need for an external amplifier circuit.

Formation of the probe element in a semiconductor die fabrication or metallisation procedure may be achieved by modification of existing masking stages or by incorporation of a new stage. An overall final metallisation layer is particularly effective as a large area maximises linkage, but this requires an extra step. Incorporation into interconnection or pad metallisation layouts is possible but may be restricted in total area due to the space required by the interconnects and/or pads. Another opportunity is to utilise metallisation or conductive layers that are incorporated for security or protective purposes, such as tamper resisting layers. Such layers as these are not connected externally in their original purpose, and are usually fragmentary islands overlying some parts of a die surface only. Modification to incorporate conductive connection to an external terminal point of the die element and, if needed, to electrically interconnect islands of conductive regions is envisaged.

As already mentioned, the on or in die location of the probe provides good capacitative linkage to the die wire bonds and any connected conductive elements including traces, signal planes and solder balls. There are two aspects to this good linkage. One is that the line of sight is unlikely to be completely obscured. Even if partly obscured some part of the probe is almost certain to be able to link to some part of each wire.

The second aspect is proximity of the probe to the wire, which in turn enables larger capacitative measurements and greater sensitivity. Typically when utilising the prior art external probes, capacitative measurements are of the general order, say, of around 20 to 200 femtofarads. In the present invention, when testing to a comparable conductive route, the reduced line of sight distance will render a larger measurement raising the previous 20 femtofarads to 40 femtofarads, and putting within resolution linkages that previously were below a useful or measurable level. The value of the capacitance measurement, compared with the expected value, can also be indicative of the nature and location of a fault.

It will be appreciated that although the invention is particularly useful for testing packages where using external probes have presented problems, the invention has general utility and

may be employed for all types of packages as the advantages of sensitivity, and also standardisation of testing practice remain.

Claims

1. A semiconductor die element (8) having active circuit elements and including a capacitative sensing probe (18) of a conductive material carried by the semiconductor die element and conductively linked to a terminal connection point.

2. A semiconductor die element according to claim 1 in which the capacitative sensing probe is formed integrally with the die element.

3. A semiconductor die element according to claim 1 or claim 2 in which the capacitative sensing probe is insulated from the active circuit elements and associated metallisation.

4. A semiconductor die element according to any preceding claim in which the terminal connection point comprises a bond pad or a trace.

5. A semiconductor die element according to any preceding claim in which the capacitative sensing probe comprises a conductive area fabricated in the surface of the semiconductor material of the die element.

6. A semiconductor die element according to any of claims 1 to 4 in which the capacitative sensing probe comprises a conductive area fabricated in a layer disposed over a surface of the semiconductor material of the die element.

7. A semiconductor die element according to claim 6 in which the layer disposed over the surface of the semiconductor material is one of: a metallisation layer, a protective layer and a tamper resistant layer.

8. A semiconductor die element according to any preceding claim in which the sensing probe forms a ring.

9. A semiconductor die element according to any preceding claim in which the probe extends at least in an area proximate and substantially all the way round a periphery of the die element surface.

10. A semiconductor die element according to any preceding claim in which the probe extends over substantially the whole upper surface of the die element.

11. A semiconductor die element according to any preceding claim in which at least part of the probe extends over a side or bottom portion of the die element.

12. A semiconductor die element according to any preceding claim further comprising an amplifier fabricated integrally with the die element and connected to the capacitative probe.

13. A semiconductor die according to any preceding claim in which the probe is located and configured with respect to bonding pads for other elements such that bonding wires (17) connected to bonding pads pass over at least part of the probe.

14. An integrated circuit package comprising:

a semiconductor die element (8);

a package having a plurality of exposed terminal conductors (15);

a plurality of conductive linkages (17) extending from the die element to the terminal conductors; and

a conductive, capacitative sensing probe (18) carried by the die element and conductively linked to an external terminal, the sensing probe being capacitatively related with respect to at least some of the conductive linkages.

15. An integrated circuit package according to claim 14 in which the package further includes at least one signal layer that embodies an electrical circuit.

16. An integrated circuit package according to claim 14 or claim 15 in which the plurality of exposed terminal conductors are selected from: a ball grid array, a lead frame and connecting pins.

17. An integrated circuit package according to any of claims 14 to 16 in which at least some of the plurality of linkages extend over at least part of the probe.

18. An integrated circuit package according to any of claims 14 to 16 in which the die element is a die element according to any of claims 1 to 13.

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Application No: GB 9927426.8 **Examiner:** SJ Morgan
Claims searched: 1-18 **Date of search:** 17 February 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K(KMA); G1U(UR31312,UR31303,UR31316)

Int Cl (Ed.7): H01L 21/66; G01R 31/303, 31/312, 31/316

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0 805 356 A2	(HEWLETT-PACKARD) See line 40, column 8 - line 31, column 12	1-11, 14-16, & 18
X	EP 0 277 764 A2	(WESTINGHOUSE) See line 28, column 4 - line 16, column 5	1, 3-7, 9-11, 14-16, & 18

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.